REMARKS

This paper is being filed together with the accompanying Request for Continued Examination. Claims 10 – 13 and 18 – 21 are being canceled. The subject matter of Claim 10 is being incorporated into Claim 6. No new matter is being added.

In a decision dated June 28, 2006, the Board affirmed the examiner's decision rejecting all of the claims on appeal, namely Claims 6 – 21, as being unpatentable under 35 U.S.C. 103(a) taking the disclosures of U.S. Patent No. 5,418,855 to Wijaranakula in view of certain pages from a book by Wolf et al (see prior citations).

Contrary to the characterization by the Board, substantial differences exist between that which is claimed and the teachings of Wolf et al. An object of the present invention is to provide a novel manufacturing process for a silicon epitaxial wafer having an IG (internal gettering) ability as set forth in lines 6 – 16 on page 4 of the application.

"0.02 Ω-cm or lower" is a preferable substrate concentration to attain the object (effect) of the present invention. Namely, as is obvious from Figure 2, using P-type silicon substrate with a resistivity of 0.016 Ω-cm and 0.008 Ω-cm, the bulk defect density is much higher than that with 10 Ω-cm after performing the heat treatment at a temperature between 450° and 750° C. On the other hand, it has been known that, using N-type silicon substrate with a resistivity of 0.02 Ω-cm or lower, oxygen is hard to be precipitated therein as set forth in line 25 on page 5 of the specification.

However, according to the present invention, even if using such an N-type silicon substrate, the bulk defect density can be increased as shown in Figures 4 and 5.

In contrast, Wolf et al only teaches a general range of resistivity which can be used to manufacture a mere normal silicon wafer. Wolf et al is silent on **increasing the bulk defect density** and having a **remarkable IG ability**. There is no suggestion or teaching that any particular benefit would be obtained by producing an epitaxial wafer with any particular resistivity.

An epitaxial wafer of Wijaranakula is useful as a calibration wafer for measurement of thickness of a microdefect-free layer (note the abstract of Wijaranakula) while an epitaxial wafer of the present invention is for a device fabrication process as set forth in paragraph 2 on page 4 of the specification. As a result, an epitaxial wafer of Wijaranakula includes a bulk region having large, uniformly distributed oxide microdefects as set forth in lines 39 – 42 of column 3. Therefore, to obtain the same, Wijaranakula teaches, after growing an epitaxial layer, the semiconductor silicon substrate is annealed at a temperature preferably between 600° and 900°C for longer than 24 hours as set forth in lines 33 – 38 of column 5.

In contrast, since an epitaxial wafer of the present invention is for a device fabrication process, in view of productivity, the heat treatment time is within 24 hours as set out in lines 14 – 19 on page 5 of the specification.

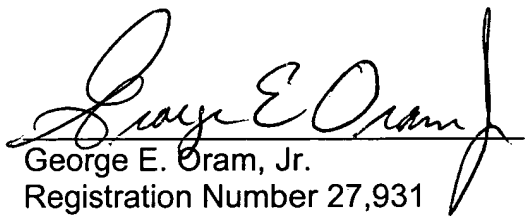
Accordingly, there is no reason that a person of skill in the art considering a process for production of a wafer for a device fabrication process would be motivated to try using the teachings of the reference. Since Wolf is silent concerning **increasing the bulk defect density** and providing a wafer having a **remarkable IG ability**, there is no reason for combining the teachings of both references.

Reconsideration by the examiner and an early examination on the merits are respectfully requested. It is respectfully contended that the present invention would not have been obvious viewing the teachings of Wijaranakula and Wolf et al.

An early Notice of Allowance is requested.

In the event that this paper is not considered to be timely filed, an appropriate extension of time is requested. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to Deposit Account No. 01-2300, referencing Attorney Docket Number 107242-00024.

Respectfully submitted,



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